METHOD AND APPARATUS FOR DECODING MULTIPLE BIT SEQUENCES THAT ARE TRANSMITTED SIMULTANEOUSLY IN A SINGLE CHANNEL

BACKGROUND OF THE INVENTION

This invention relates to communication systems; and more particularly, it relates to methods and apparatus for decoding multiple bit sequences that are transmitted simultaneously and asynchronously to a receiving station over a single channel in which the bit sequences are added.

Conventionally, when multiple bit sequences are transmitted at the same time to a receiver, each of the bit sequences is transmitted on a separate channel. In that case, the bit sequences of the separate channels do not interfere with each other. Thus the receiving station can simply filter the signals that are in one channel from the signals that are in the other channels. However, such a system has an inherent deficiency in that it requires multiple communication channels, which in certain instances are not available.

By comparison, with the present invention, multiple bit sequences are sent simultaneously to a receiver over a single channel. In this channel, the bit sequences are added together and thereby form a composite signal which is what the receiver sees. Thus, it is the task of the receiver to decode or recover the bit sequences from which the composite signal was formed.

This decoding problem is addressed in a prior art paper entitled "Minimum Probability of Error for Asynchronous Gaussian Multiple Access Channels" by S. Verdu, *IEEE Transactions on Information Theory*, IT-32, pp. 85–96, January 1986. In that paper, a decoding procedure is presented which uses a bank of K matched filters (where K is the number of bit sequences that are simultaneously transmitted in the composite signal), followed by a metric evaluation process. However, the Verdu procedure requires a total of 2^K metric calculations for each bit in the composite signal that is decoded; and such exponential dependence on the number of bit sequences in the composite signal makes the Verdu decoder too complex to implement, even for a moderate number of users.

Accordingly, a primary object of the present invention is to provide another decoding procedure, as well as circuitry for carrying out that procedure, which is only linearly dependent on the number of bit sequences that are in the composite signal.

BRIEF SUMMARY OF THE INVENTION

Using the present invention, data bits are decoded from a composite signal that is formed by coding K bit sequences with respective spreading codes, and transmitting the coded bit sequences simultaneously and asynchronously over a single channel in which the bit sequences are added. This decoding, in accordance with the invention, includes the following steps:

(1) comparing the content of several registers, each of which contains a particular bit sequence and a metric for that sequence, to determine the largest metric M_{max} and the corresponding bit sequence b_s;

(2) evaluating a new pair of metrics for the very next bit b(x) which follows the bit sequence b_s by using estimated "0" and "1" values for bit b(x), K-1 bits from the sequence b_s which immediately precede bit b(x), and matched filter outputs for K-1 bits in the composite signal which immediately follow bit b(x); and

(3) replacing the register which contains the bit sequence b_s with two registers, one of which contains the bit sequence $b_s b(x)=0$ and the metric M_{max} plus the above evaluated metric for $b(x)=0$, and the other of which contains the bit sequence $b_s b(x)=1$ and the metric M_{max} plus the above evaluated metric for $b(x)=1$.

Steps 1, 2, and 3 are repeated multiple times; and thereafter, the composite signal is decoded as the bit sequence in the register which contains the largest metric. With this method, a sequence of N bits in the composite signal will, on average, be decoded by performing steps 1, 2, and 3 a total of N times.

BRIEF DESCRIPTION OF THE DRAWINGS

Various features and advantages of the invention are described herein in conjunction with the accompanying drawings wherein:

FIG. **1** illustrates a communication system in which the present invention is incorporated;

FIG. **2** illustrates the details of one of the bit sequences in the FIG. **1** system;

FIG. **3** illustrates how the multiple bit sequences in the FIG. **1** system are combined to form a composite signal at the receiving station;

FIG. **4** gives a preferred metric for the receiver in the FIG. **1** system to use in decoding the composite signal;

FIG. **5** illustrates the sequence by which the FIG. **4** metric is used by the receiving station to decode the composite signal;

FIG. **6** gives actual bit sequences and spreading codes that were used to form a composite signal in a computer simulation of the disclosed decoding procedure;

FIG. **7** gives matched filter outputs and cross correlations which resulted from the computer simulation of the FIG. **6** bit sequences;

FIG. **8** shows the remaining portion of the decoding procedure that was computer simulated in accordance with FIGS. **4** and **5**;

FIG. **9** shows a decoder which performs the decoding process of FIGS. **4** and **5**; and

FIG. **10** shows additional details of the metric circuit in the FIG. **9** decoder.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to FIG. **1**, it shows an overall view of a communications system in which the invention is used. In this illustrated communications system, there are four transmitting stations T_1, T_2, T_3, and T_4 and one receiving station R. Each station may be housed within any suitable mechanism, such as an airplane or satellite, for example.

Station T_1 communicates with station R by sending a coded sequence of data bits which is indicated in FIG. **1** as a sequence s_1. In that sequence, the symbols $b_1(0)$, $b_1(1)$, $b_1(2)$, $b_1(3)$, . . . represent uncoded data bits, and the symbol a_1 represents a spreading code which is multiplied by each of the uncoded data bits prior to their transmission.

Similarly in FIG. **1**, the symbols s_2, s_3, and s_4 respectively indicate coded bit sequences which are sent by the transmitting stations T_2, T_3 and T_4. Each bit in signal s_2 is multiplied by a spreading code a_2; each bit in signal $s_3$is multiplied by a spreading code a_3; and each bit in signal s_4 is multiplied by a spreading code a_4.